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Embedded Real-Time FPGA Signal Processing Strategies

Embedded Tech Trends 2013

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Challenges for Embedded FPGA DSP

High-speed A/D and D/A Interfaces
A/D sampling rates of > 3 GHz

Digital Up and Down Conversion
Baseband signals simplifies DSP algorithms

Fast System Interfaces
Eliminate real-time data flow bottlenecks

Multi-Channel Synchronization
Triggering for phased array antennas & beamforming

Large, Fast External SDRAM Buffers
Capturing transients, buffering and digital delays

FPGA Power Reduction
Silicon process, clock gating, low voltage

Board Level Power Management
Monitoring facilities for thermal performance

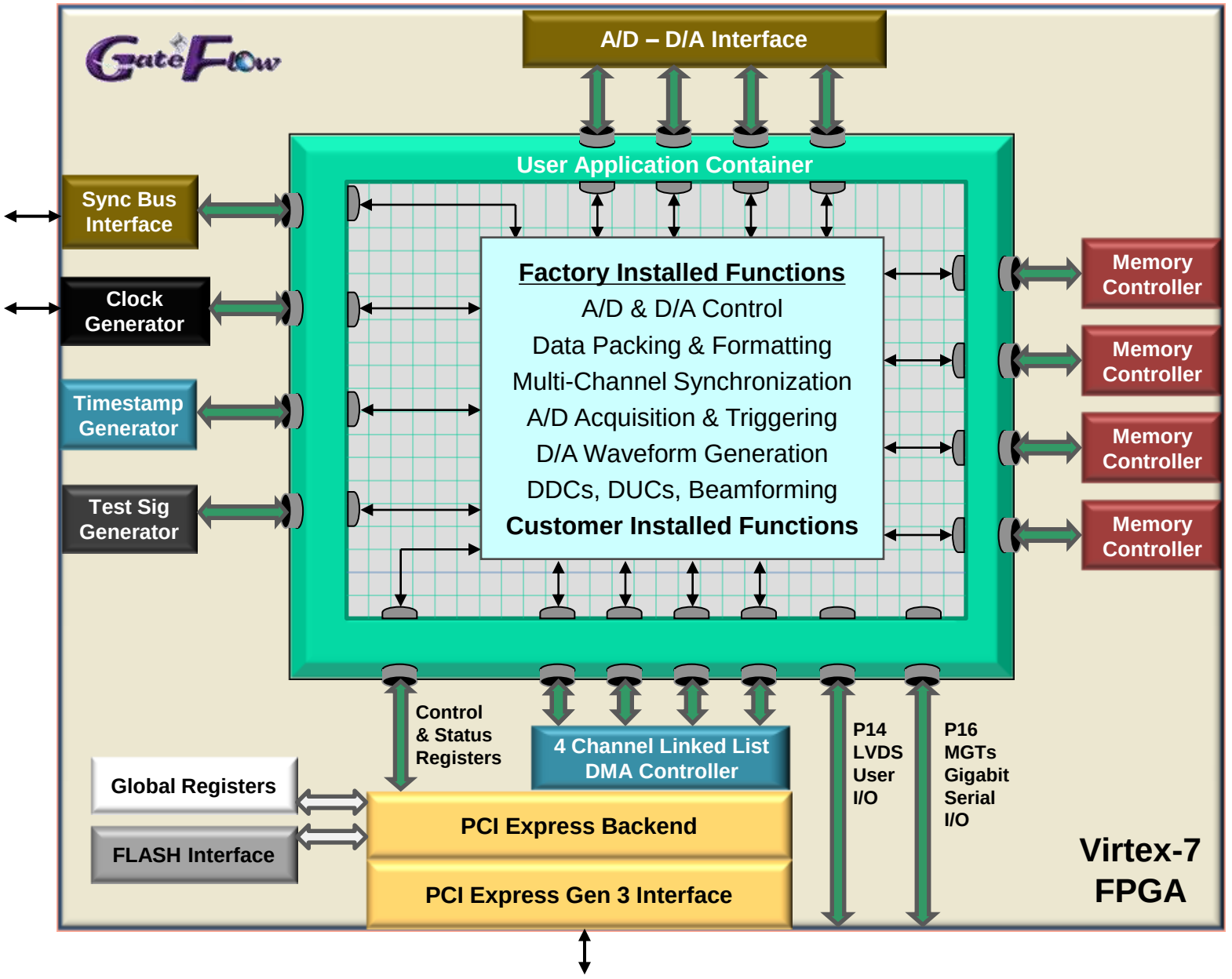
Reconfiguration of FPGAs via PCIe
CPU reconfigures FPGA during runtime

Multiple Strategies
Are Required

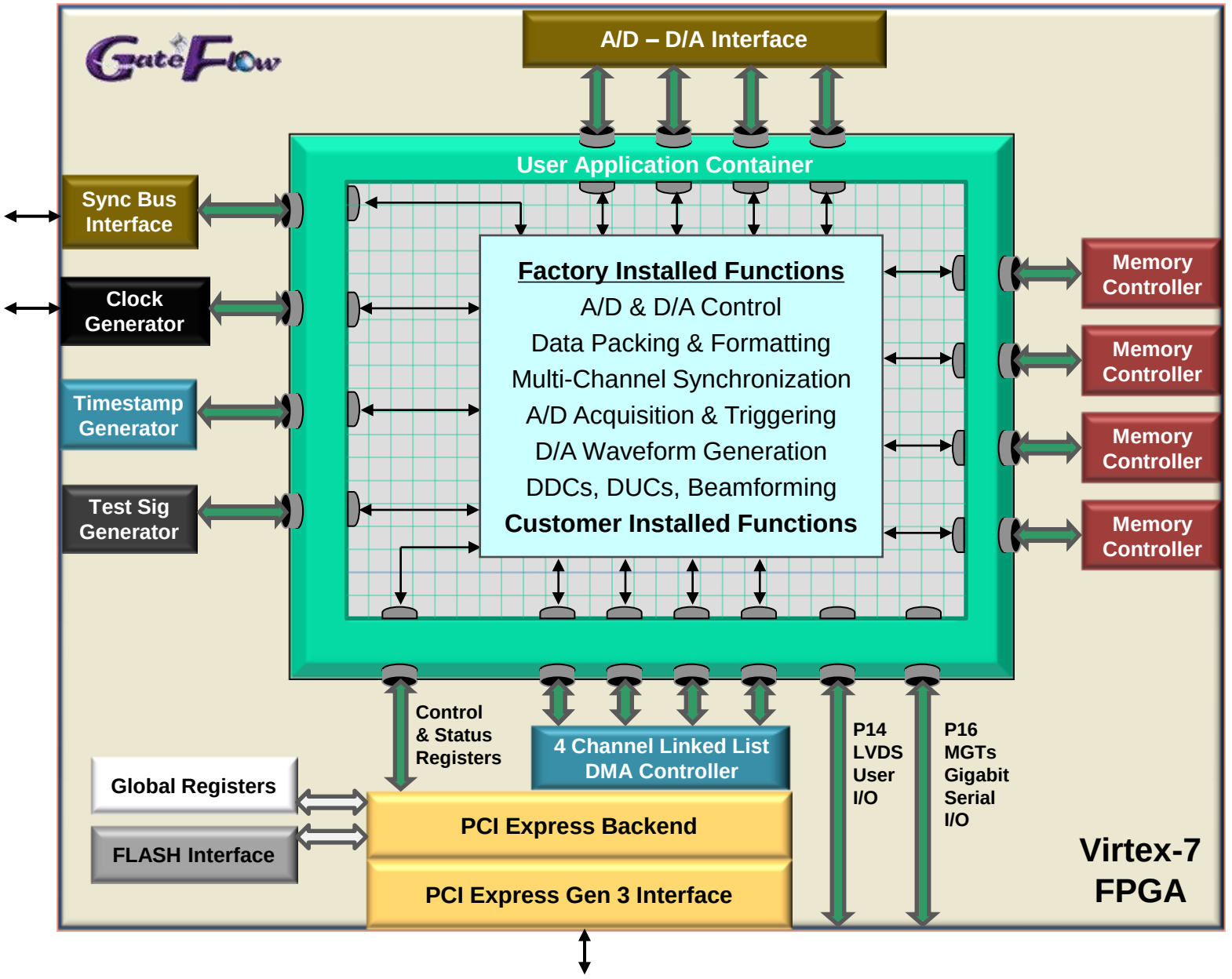
Model 71741 3.6 GHz A/D + DDC

- A/D
  - Texas Inst ADC12D1800
  - Single channel mode
    - 3.6 GHz, 12-bit
  - Dual channel mode
    - 1.8 GHz, 12-bit
- Memory Buffering
  - Real-time capture to SDRAM at 25.6 GB/sec
- Wideband Digital Down Converter
  - Mixer Translates RF to baseband
  - FIR Filter sets baseband bandwidth
  - Output bandwidths to 360 MHz

Pentek FPGA Organization

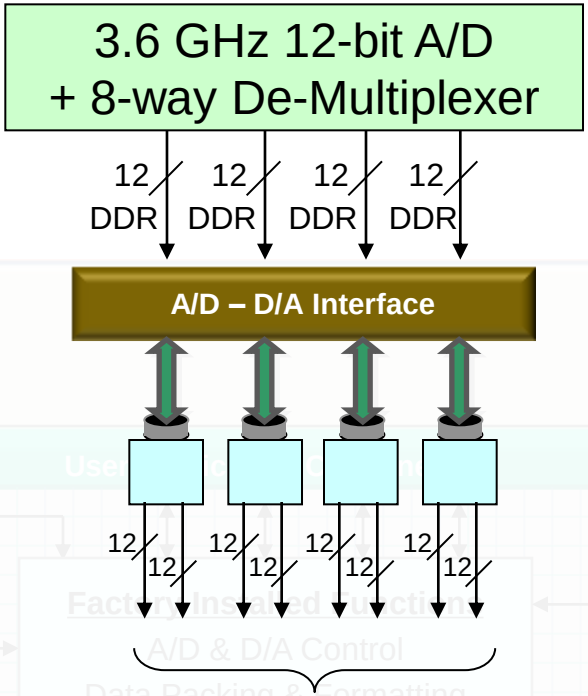


Pentek FPGA Organization



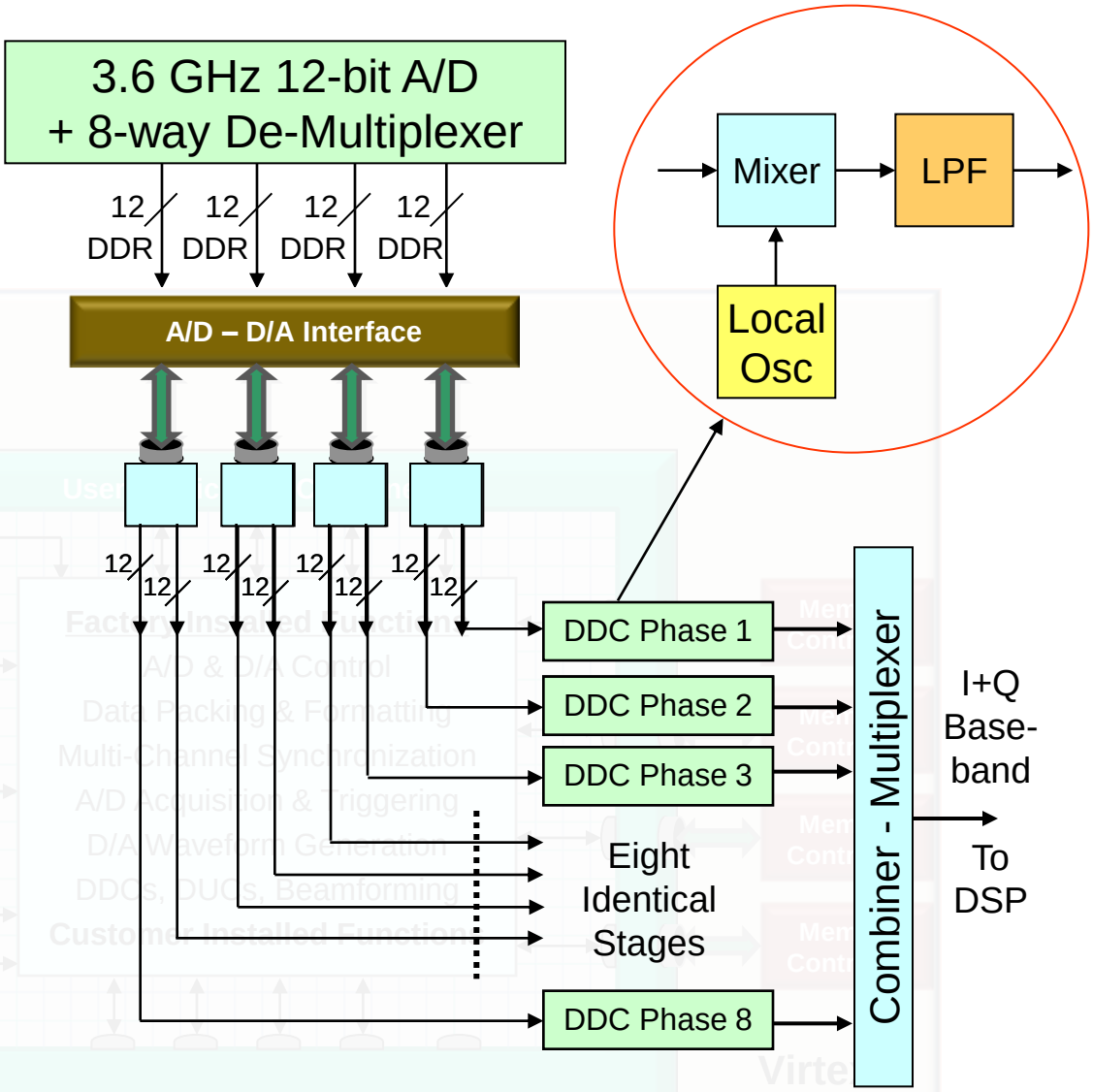
3.6 GHz Digital Down Converter

- FPGAs can handle signal streams for DSP processing only up to about 500 MHz
- 3.6 GHz 12-bit A/D has four LVDS DDR 12-bit output buses
- FPGA LVDS I/O ports handle DDR mode to 1 GHz or more
- Creates eight 12-bit streams at 450 MHz - ready for DSP

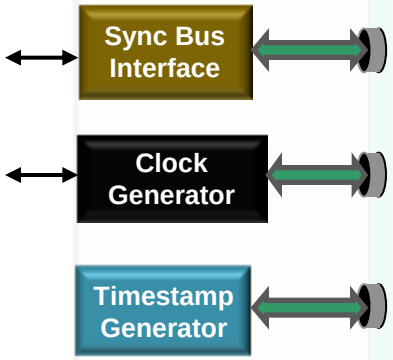


3.6 GHz Digital Down Converter

- Eight polyphase DDC IP cores each operate in parallel at 450 MHz
- Each DDC core contains its own local oscillator, mixer and low pass filter
- Tuning range from DC to 3.6 GHz
- Output bandwidth is programmable from 90 to 360 MHz BW
- DDC outputs are multiplexed to a single baseband I+Q stream
- Signals ready for delivery to DSP algorithms



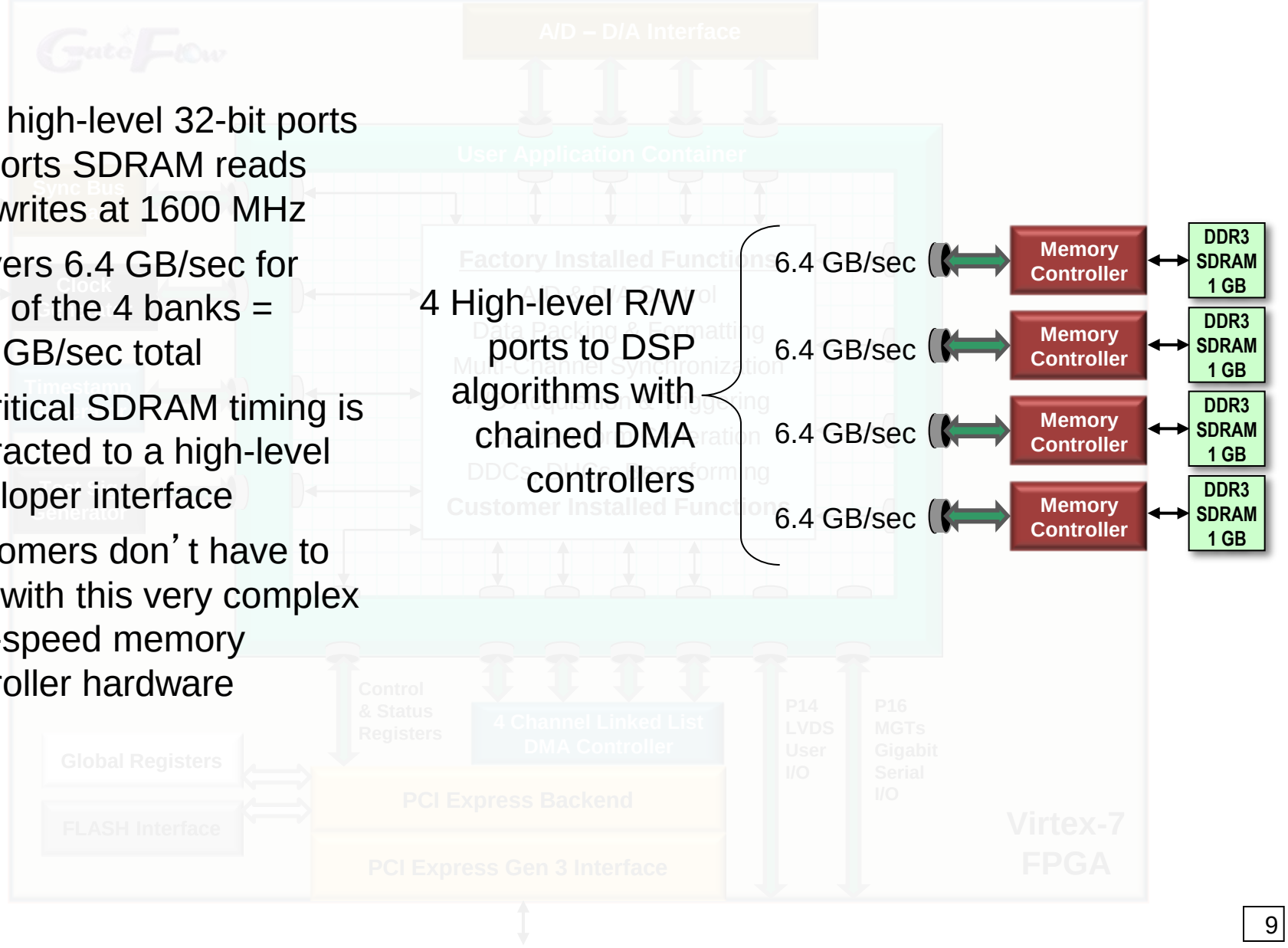
Multi-Channel Synchronization



- Sync bus synchronizes clocking, gating, triggering across multiple modules
- Time stamping of each captured block with support for GPS receiver
- Dozens of different clock/sync generator products supports systems with hundreds of channels
- Synchronous operation between A/Ds, DDCs, DUCs, and D/As
- On-board frequency synthesizers accept external 10 MHz reference
- Simplifies data acquisition, waveform generation, synchronization and timing tasks for DSP application developers

1600 MHz DDR3 SDRAMs

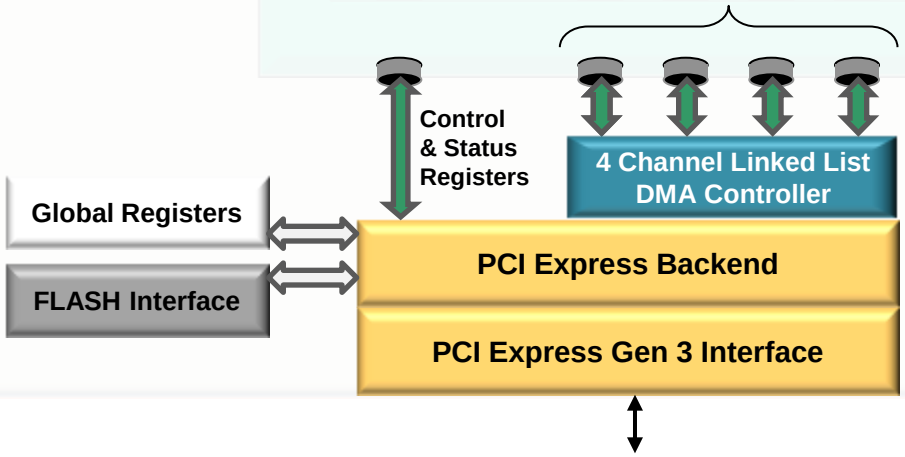
- Four high-level 32-bit ports supports SDRAM reads and writes at 1600 MHz
- Delivers 6.4 GB/sec for each of the 4 banks = 25.6 GB/sec total
- All critical SDRAM timing is abstracted to a high-level developer interface
- Customers don't have to deal with this very complex high-speed memory controller hardware



Gen 3 PCIe System Interface

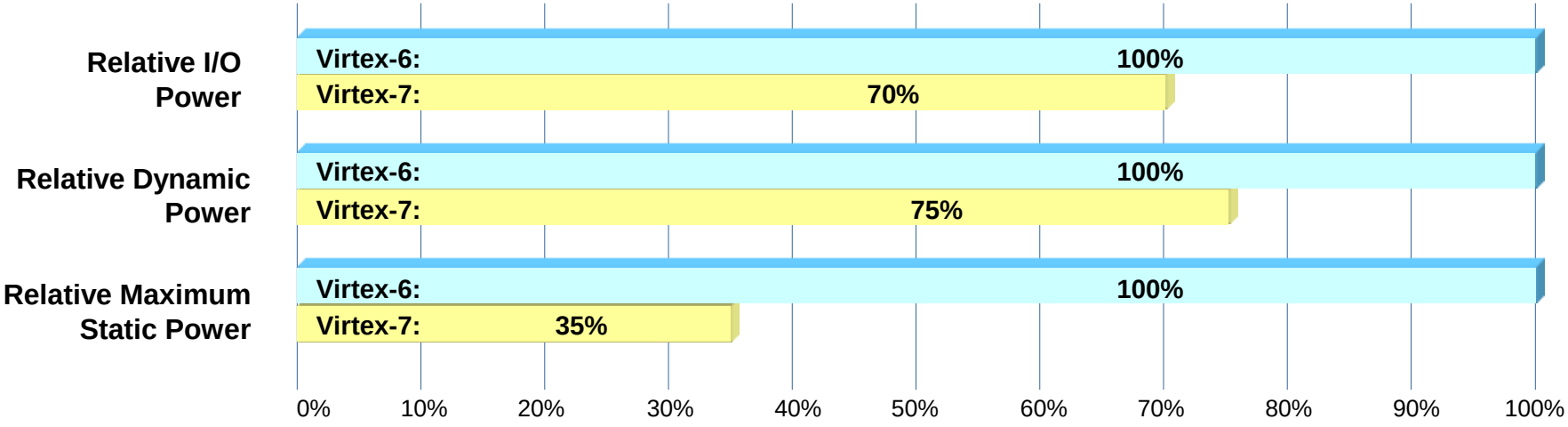
- Four high-level streaming 32-bit data ports to PCIe
- Aggregate rates up to 8 GB/sec with x8 PCIe Gen 3
- Chaining DMA controllers simplify data transfers to system RAM
- Supports data buffer architectures for complex applications

4 high-level FIFO Data Ports
with 4 independent chained
DMA Controllers



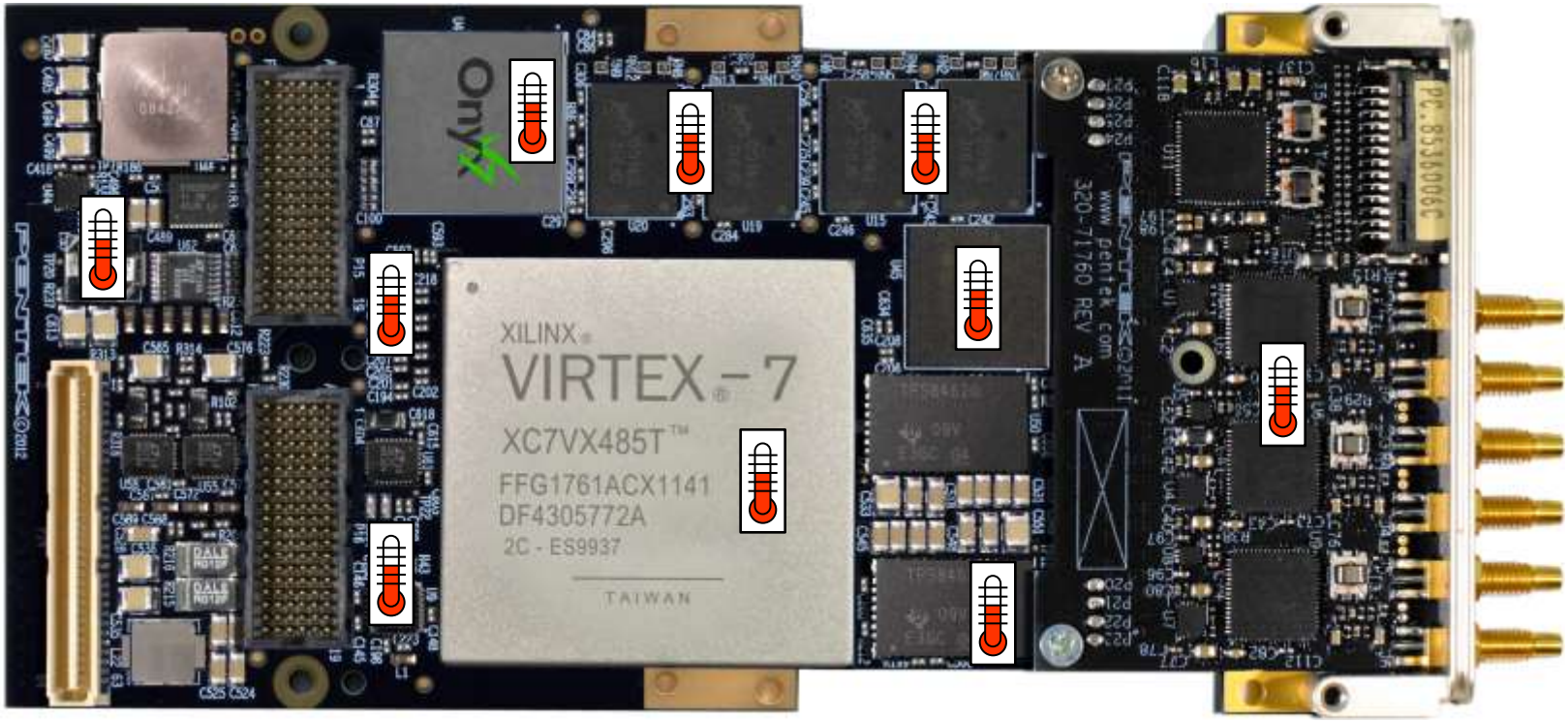
Xilinx Virtex-7 FPGA Power Reduction

- 28nm HPL Process
  - Optimized blend of high-performance and low-power HKMG technology
- Advanced on-chip clock gating eliminates clocking of unused logic
- Voltage Scaling
  - Allows power supply voltage reduction on graded devices
- Integrated blocks - more efficient than fabric implementations
- Stacked Silicon Interconnect technology saves I/O power
- Power Efficient modes for gigabit serial transceivers



Onyx Temperature Monitoring

- 10 on-board temperature sensors
- Helps validate thermal management designs
- Useful during development and deployment

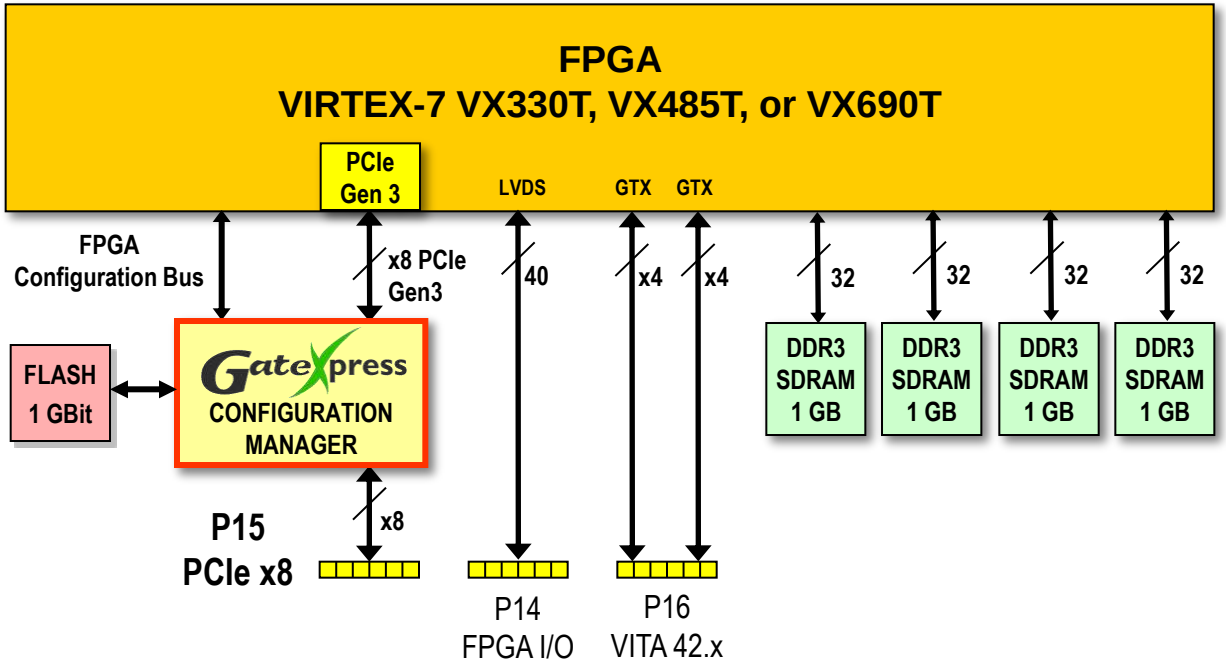


Onyx Voltage & Power Monitoring

- 9 on-board voltmeters monitor critical power supplies
- 2 on-board ammeters measure both 5/12V and 3.3V supply current
- Allows direct measurement of power consumption
- Programmable thresholds can send interrupts to system CPU

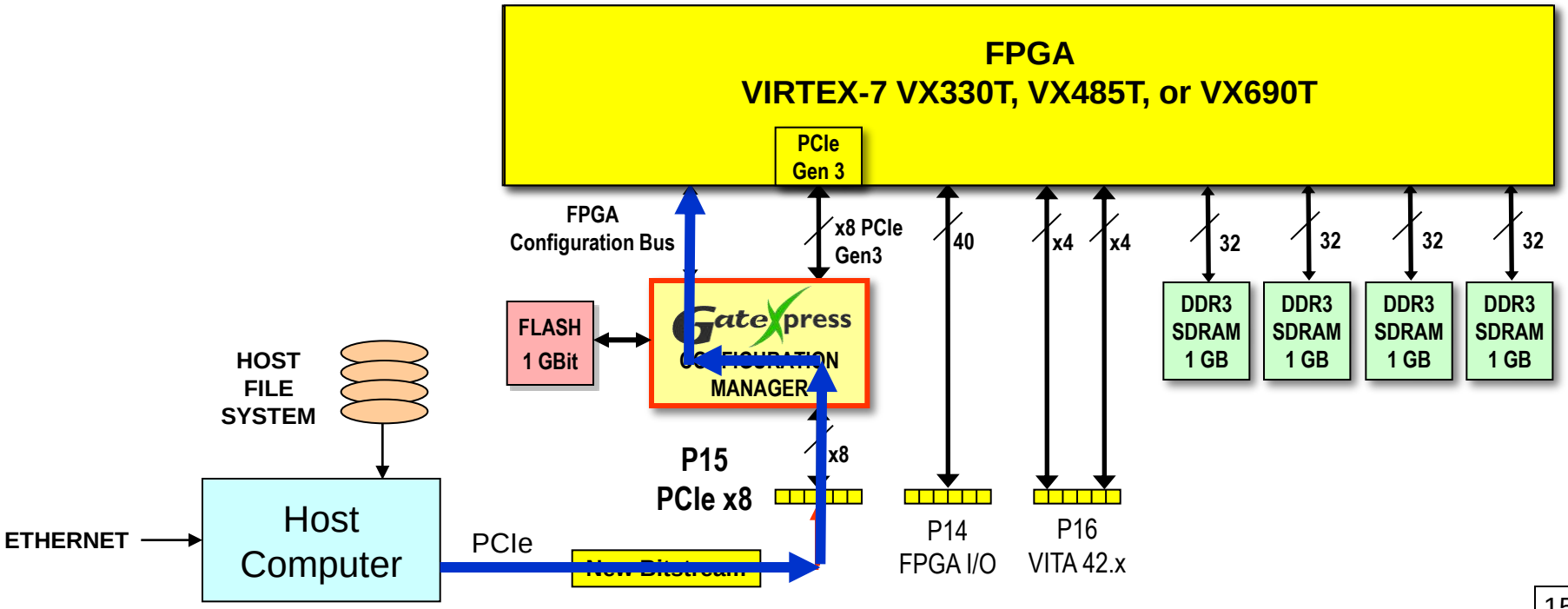
GateXpress PCIe Configuration Manager

- Larger FPGAs take a long time to initialize from power up
  - PCIe systems scan for devices within 100 ms after power
  - System must be soft rebooted to repeat PCIe enumeration
- GateXpress manager presents a simple PCIe interface immediately
- PCIe configuration space parameters are saved for the Virtex-7
- Eliminates need for rebooting at power up



GateXpress PCIe Configuration Manager

- Allows host software utility to completely reconfigure the entire FPGA
- All loading done through the host PCIe interface with no reboot
- Preserves all PCIe configuration space parameters
- Eliminates J-TAG cables during development
- Supports live, run-time FPGA reconfiguration without reboot



Embedded FPGA DSP Strategies

- Modular organization of FPGA IP resources allows easy modification or addition of new signal processing IP
- Offer an FPGA Design Kit so customers can extend & modify the FPGA functions for custom algorithms
- Provide rich infrastructure of standard FPGA resources fully supported with board support libraries
- Offer high-performance factory installed IP cores for popular DSP functions like digital downconverters
- Take advantage of Virtex-7 power reduction
- Provide resources for monitoring temperature, voltage and current during development and deployment
- GateXpress PCIe Configuration manager allows recon-figuration of FPGA across PCIe with no system reboot
- Allows FPGA designers to concentrate on their value-added, application-specific proprietary IP
- Visit www.pentek.com for more details